WHAT IS CLAIMED IS:

1   1.   A pipeline accelerator, comprising:

2   a communication bus; and

3   a plurality of pipeline units each coupled to the communication bus and each

4   comprising a respective hardwired-pipeline circuit.

1   2.   The pipeline accelerator of claim 1 wherein each of the pipeline units

2   comprises:

3   a respective memory coupled to the hardwired-pipeline circuit; and

4   wherein the hardwired-pipeline circuit is operable to,

5   receive data from the communication bus,

6   load the data into the memory,

7   retrieve the data from the memory,

8   process the retrieved data, and

9   drive the processed data onto the communication bus.

1   3.   The pipeline accelerator of claim 1 wherein each of the pipeline units

2   comprises:

3   a respective memory coupled to the hardwired-pipeline circuit; and

4   wherein the hardwired-pipeline circuit is operable to,

5   receive data from the communication bus,

6   process the data,

7   load the processed data into the memory,

8   retrieve the processed data from the memory, and

9   load the retrieved data onto the communication bus.

1   4.   The pipeline accelerator of claim 1 wherein each of the hardwired-pipeline

2   circuits is disposed on a respective field-programmable gate array.

1   5.   The pipeline accelerator of claim 1, further comprising:

2   a pipeline bus; and

3   a pipeline-bus interface coupled to the communication bus and to the pipeline

4   bus.

1   6.   The pipeline accelerator of claim 1, further comprising:

2   wherein the communication bus comprises a plurality of branches, a respective

3   branch coupled to each pipeline unit; and

4   a router coupled to each of the branches.

1   7.   The pipeline accelerator of claim 1, further comprising:

2   wherein the communication bus comprises a plurality of branches, a respective

3   branch coupled to each pipeline unit;

4   a router coupled to each of the branches;

5   a pipeline bus; and

6   a pipeline-bus interface coupled to the router and to the pipeline bus.

1   8.   The pipeline accelerator of claim 1, further comprising:

2   wherein the communication bus comprises a plurality of branches, a respective

3   branch coupled to each pipeline unit;

4   a router coupled to each of the branches;

5   a pipeline bus;

6   a pipeline-bus interface coupled to the router and to the pipeline bus; and

7   a secondary bus coupled to the router.

1   9.   The pipeline accelerator of claim 1 wherein:

2   the communication bus is operable to receive data addressed to one of the

3   pipeline units; and

4   the one pipeline circuit is operable to accept the data; and

5   the other pipeline circuits are operable to reject the data.

1   10.   The pipeline accelerator of claim 1, further comprising:

2   wherein the communication bus comprises a plurality of branches, a respective

3   branch coupled to each pipeline unit;

4   a router coupled to each of the branches and operable to,

5   receive data addressed to one of the pipeline units, and

6   provide the data to the one pipeline unit via the respective branch of the

7   communication bus.

1   11.   A computing machine, comprising:

2   a processor;

3   a pipeline bus coupled to the processor; and

4   a pipeline accelerator comprising,

5   a communication bus,

6   a pipeline-bus interface coupled between the pipeline bus and the

7   communication bus, and

8   a plurality of pipeline units each coupled to the communication bus and

9   each comprising a respective hardwired-pipeline circuit.

1   12.   The computing machine of clam 11 wherein:

2   the processor is operable to generate a message that identifies one of the

3   pipeline units and to drive the message onto the pipeline bus;

4   the pipeline-bus interface is operable to couple the message to the

5   communication bus;

6   the pipeline units are each operable to analyze the message;

7   the identified pipeline unit is operable to accept the message; and

8   the other pipeline circuits are operable to reject the message.

1   13.   The computing machine of claim 11, further comprising:

2   wherein the communication bus comprises a plurality of branches, a respective

3   branch coupled to each pipeline unit;

4   wherein the processor is operable to generate a message that identifies one of

5   the pipeline units and to drive the message onto the pipeline bus; and

6   a router coupled to each of the branches and to the pipeline-bus interface and

7   operable to receive the message from the pipeline-bus interface and to provide the

8   message to the identified pipeline unit.

1   14.   The computing machine of claim 11, further comprising:

2   wherein the communication bus comprises a plurality of branches, a respective

3   branch coupled to each pipeline unit;

4   a secondary bus; and

5 a router coupled to each of the branches, to the pipeline-bus interface, and to the

6 secondary bus.

1 15. A method, comprising:

2 sending data to first of a plurality of pipeline units via a communication bus, each

3 pipeline unit including a respective hardwired pipeline; and

4 processing the data with the first pipeline unit.

1 16. The method of claim 15 wherein sending the data comprises:

2 sending the data to a router; and

3 providing the data to the first pipeline unit with the router via a respective first

4 branch of the communication bus.

1 17. The method of claim 15 wherein sending the data comprises sending the

2 data to the first pipeline unit with a processor.

1 18. The method of claim 15 wherein sending the data comprises sending the

2 data to the first pipeline with a second of the plurality of pipeline units.

1 19. The method of claim 15, further comprising driving the processed data

2 onto the communication bus with the first pipeline unit.

1 20. The method of claim 15 wherein processing the data with the first pipeline

2 unit comprises:

3 receiving the data from the communication bus with a hardwired-pipeline circuit,

4 loading the data into a memory with the hardwired-pipeline circuit,

5 retrieving the data from the memory with the hardwired-pipeline circuit, and

6 processing the retrieved data with the hardwired-pipeline circuit.

1 21. The method of claim 15, further comprising:

2 wherein processing the data with the first pipeline unit comprises,

3 receiving the data from the communication bus with a hardwired-pipeline

4 circuit,

5 processing the received data with the hardwired-pipeline circuit, and

6   loading the processed data into a memory with the hardwired-pipeline

7   circuit; and

8   retrieving the processed data from the memory and driving the processed data

9   onto the communication bus with the hardwired-pipeline circuit.

1   22.   The method of clam 15, further comprising:

2   generating a message that includes the data and that identifies the first pipeline

3   unit as a recipient of the message; and

4   wherein sending the data to the first pipeline unit comprises determining from the

5   message that the first pipeline is a recipient of the message.

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